TEMPEST PC Board Design

Chapter 8

Introduction

Source suppression at the board level has always been the "ideal" solution to not only TEMPEST, but to other EMC related design problems as well. If the design engineer is able to physically place IC' s or other devices with high frequency emission characteristics away from other devices, can choose the location of the interconnect, power, and ground configurations, and if the designer can then select the number of pc board layers that will be used, then many of the problems associated with board emissions can be solved directly.

Building "quiet" boards from the start is a relatively simple process. However, the most common case experienced by TEMPEST designers is the case where a circuit board is already built, and modifications are necessary to reduce problem emanations. In this situation, unless a small vector board is to be piggyback mounted to the original board, little additional suppression can be done to the existing board other then trace cuts, adding components, and changing components to different values or families.

Designing From the Start

Occasionally the need arises to build a new card or re-layout an existing card, especially in the computer industry. If a card is to be redesigned, the TEMPEST designer must get involved early in the process in order to insure the new card can effectively meet whatever emission controls may be imposed. It is in this regard that the following information and techniques will prove most useful.

Begin the project by carefully comparing the logic families selected against the signal or circuit constraints on the design. Obviously if a low noise CMOS device can be used in a sensitive signal path instead of a noisy low power Shottky device, then the CMOS device should be substituted.

Next, look for the presence or absence of primary emission sources such as buffered oscillators and microprocessors. These devices are intended to source large high frequency currents and will also have the shortest transition times. Electromagnetic emissions are directly proportional to operating frequency and output current and inversely proportional to rise and fall times.

$$Emissions \propto \frac{FI}{t}$$

where: F = pulse repetition frequency

I = output current

t = rise/fall time (whichever is shorter)

The next area to examine before addressing the board layout is the existence of noise on the pc board's power and ground system. Input current to the board, and also to any particular IC is usually very dirty. While most commercial power supply designers, because of FCC requirements, are quick to provide filtering to prevent noise from getting

to the outside world, few (except for high frequency switchers) use other then the design's ripple rejection characteristics to reduce output noise. With the push for higher efficiency, even less noise suppression can be tolerated. In a TEMPEST suppressed environment, noise reaching a sensitive IC via either the power or the ground path can result in emission problems not only difficult to solve, but also usually difficult to find.

In the past, noisy power or ground planes or lines could be tolerated by saturating logic devices. However, the preferred practice of connecting unused input and/or output lines to the power or ground plane depending on manufacturers preference sometimes aggravated the noise problem in the plane itself. Decoupling each IC with a capacitor was an attempt to prevent false gating due to noisy power and ground systems. Current sensitive designs often provide additional linear regulation, such as a 3-terminal regulator, at the board level to reduce the presence of noise driving into the board through the power system. The final area to look at is 'aspect ratio. The best (least noisy) aspect ratio for a pc board is one, length and width equal. The higher the aspect ratio, the more likely emissions from the board will occur.

Trace Optimization

Allowable trace length for a specific signal line is directly related to the characteristic impedance of the trace, the signaling rate required, the distance to the receiving load, and the logic family and packages being used. In addition, TEMPEST and EMI engineers are also concerned with coupling between traces, common mode signals coupling into the ground plane, and the effects of the trace/device formed antenna in reducing radiated emissions.

If the circuit board trace is envisioned as a transmission line with multiple impedances mismatches created at change of direction locations, size changes, or at the pins for each IC, it is easy to imagine that many high frequency radiating points exist on every circuit trace. Therefore, the objective of a board layout effort is to either impedance match or load each transmission line over the widest range of frequencies where energy exists that could radiated to the outside world, to reduce each possible antenna to its minimum possible length, and finally to insure trace lines carrying sensitive signals are isolated such that they can not be coupled to less sensitive adjacent lines through the ground plane or via capacitive paths. Potential problem paths are shown in Figure 8-1.

Figure 8-2 shows the technique for reducing the high frequency impedance mismatch associated with a circuit trace changing direction. The propagating wave of the higher frequency harmonics associated with digital transitions reflects less energy from the rounded trace then would be the case with an abrupt direction change.

The principle method of preventing or reducing signal line ringing is through a change in current flow by reduced or increased loading using reflection, shunting, or absorption. Reflection could be employed. in the form of a series resistor or inductor with shunting, shunting would take place with capacitive or R-C loading, and absorption would result from using a series ferrite bead. Obviously, if additional damping (loading through one of the techniques shown in Figure 8-3) is added to reduce the high frequency components of the signal propagating down the trace, the reflected signal can be further reduced to prevent much of the potential for radiated emissions production.

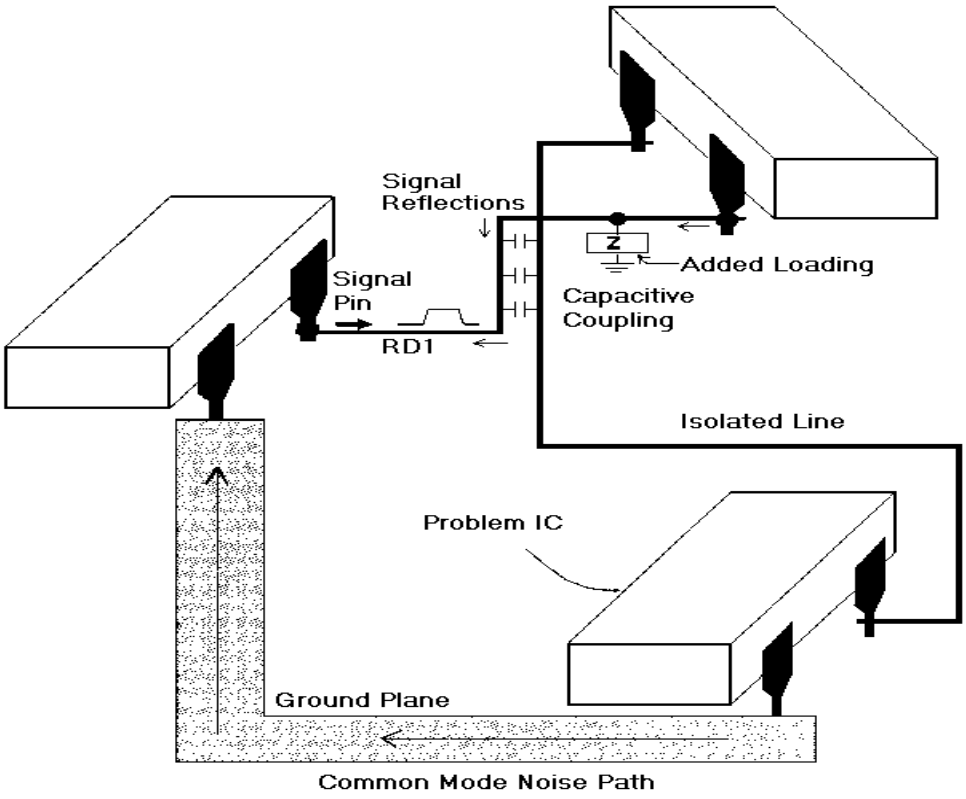


Figure 8-1 Potential Problem Paths

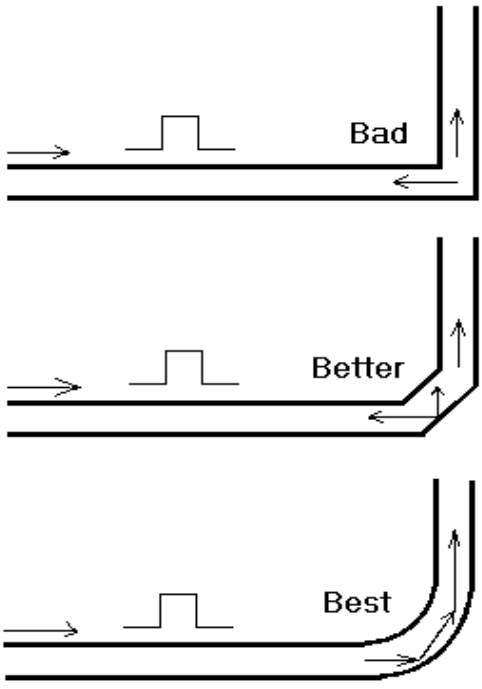


Figure 8-2 Techniques for Reducing Z Mismatch from Trace

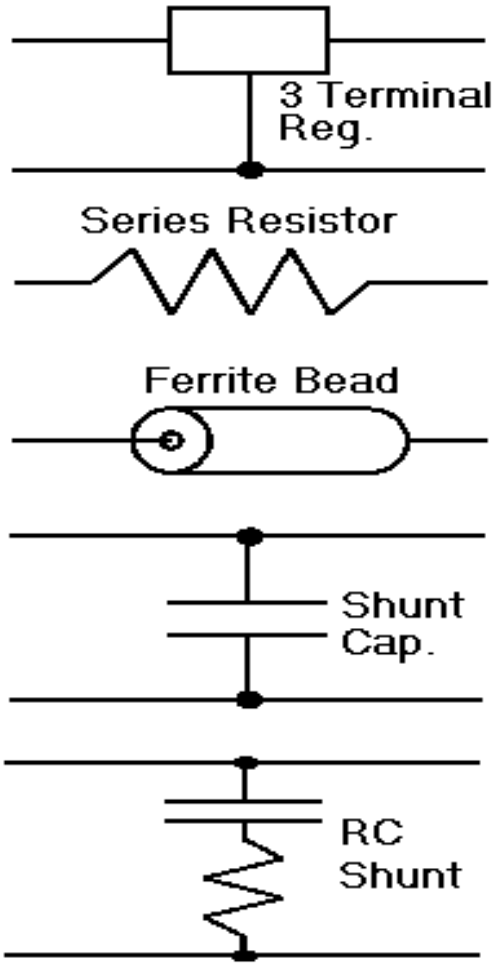


Figure 8-3 Most Common Damping Approaches

The general rule is to always reduce current as much as possible. Therefore, series resistive loading offers the best approach to eliminate noise at its source. Capacitive loading directly between the transmission line and the ground plane is a simple fix to employ, but has the tendency to drive sensitive baseband signals into the ground system, as well as overloading the current source (the IC). Note that the capacitive loading mentioned here is not the same as the capacitive decoupling used between power and ground at the IC. If increased loading is required, a better approach is to use a tuned series R-C filter to only load the high frequency components of the transmitted signal. The series ferrite is similar to the series resistor, except that it is primarily intended for the high frequency components (above 100 MHz) of the transmitted signal. For very fast logic, the series resistor should be tried initially, then the ferrite, then loading.

Microstrip techniques were developed for the microwave industry as a means of providing high frequency isolation on single sided and multilayer circuit boards. The microstrip transmission line configuration is shown in Figure 8-4. Basically, the technique involves the routing of a narrow conductor of accurately controlled width on a circuit board with ground plane below the trace.

The characteristic impedance of a microstrip conductor is found from:

$$Z_o = \frac{h}{w}\frac{377}{\sqrt{e_{(r)}}} \quad \text{in ohms}$$

where h is height, w is width, and e(r) is permeability.

However, Young (1) has modified this equation to take into account the effects of fringing at the edges of the trace. The modification is shown below.

$$Z_o = \frac{h}{w}\frac{377}{\sqrt{e_{(r)}}}\frac{1}{(1+2h)[1+\ln(\frac{w}{h})]} \quad \text{in ohms)}$$

Figure 8-5 shows the capacitive coupling between a circuit trace and two adjacent traces above a ground plane for the microstrip configuration.

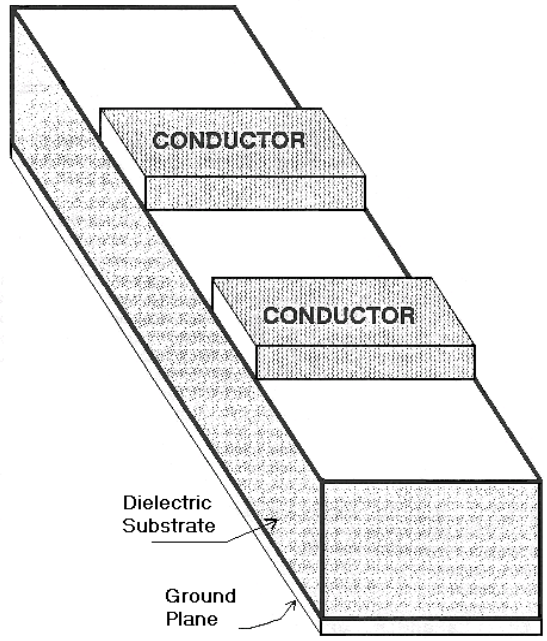


Figure 8-4 Microstrip Transmission Line

One final comment on all trace routing is in order. For multilayer TEMPEST boards, individual trace layers are best routed at right angles to each other. In addition, while standard board layout techniques call for routing as much of the interconnect under the DIP package as possible, this approach is not recommended in TEMPEST or EMI applications. DIP packages are exceedingly noisy and result in acting as a source of emissions for most logic families. Therefore, routing a circuit trace under a DIP package will not only increase signal coupling to (or from) the trace, but might also make suppressing the signal directly at its source much more difficult then would be the case if the trace was fully exposed.

Multilayer Circuit Boards

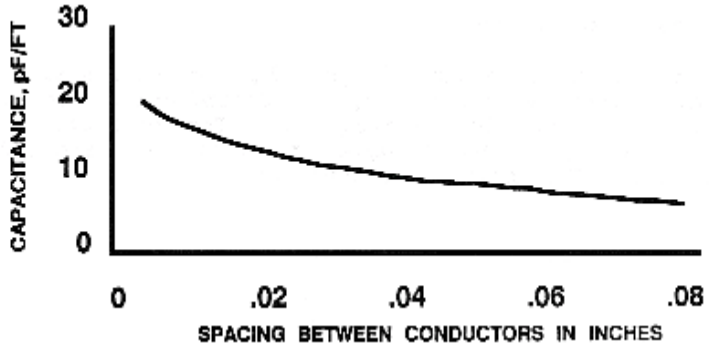


Figure 8-5 Capacitive Coupling Between Adjacent Traces

Multilayer circuit boards offer a significant increase in emission protection at high operating frequencies when compared to single or double sided circuit boards for three reasons. First, since interconnecting traces can be routed on layers other than the layer that has the components mounted to it, the components can be located physically closer, thus allowing increased density and reduced trace length. Secondly, critical or sensitive traces can be routed perpendicular, as mentioned previously, which reduces capacitive coupling. Third, ground, signal return, and power planes can nearly always be employed in multi-layer designs.

Not only do multiple ground planes provide a low impedance return path to ground, but they also allow the important capability to fully sandwich all internal layers for maximum emission control if necessary. Figure 8-6 shows one possible multilayer pc board design. Multilayer board configurations can range from 3 to 12 layers depending on density and materials used.

All components, and possibly some control type signal traces are found on layer A. Layer B is a ground plane isolating the radiating dipole antennas associated with DIP packages from the rest of the trace layers. The thickness and type of metal used for the ground plane controls the attenuation provided between the component and first trace layer. Similarly, successive ground planes between other trace layers would significantly reduce coupling between applicable adjacent trace planes.

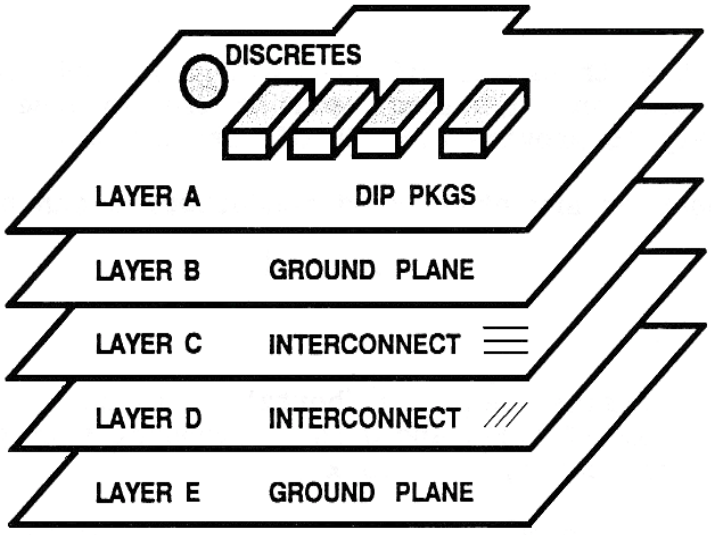


Figure 8-6 Typical PC Board Sandwich Configuration

Ground Plane Attenuation

The thickness of copper foil ground planes varies according to the isolation required between layers. Ground planes are specified by weight per square foot (oz/sq ft). The most commonly used weights are 1, 2, 3, and 4 oz/sq ft, generally referred to as simply ounces.

Thickness per ounce	
oz/sq ft .	µ meters
1	35
2	71
3	106
4	143

The signal attenuation characteristics of various thicknesses of copper foil ground plane is found by first determining the frequency of the coupling signal, and then by calculating the resulting attenuation using the following formula:

$$Attenuation(dB) = 20\log e^{-az}$$

where z is the thickness of the plane in meters, a is the attenuation constant (1/meters) and is the inverse of the skin depth necessary to provide 8.69 db of attenuation.

For copper or any other good conductor, a can be calculated as:

$$a = (\pi f \mu g)^{\frac{1}{2}}$$

where f is the signal frequency (hertz), u is the permeability of free space (4 x 10E-7 h/m), and g is the conductivity of the ground plane metal (for copper, g = 5.5 x 10E7 s/m).

Combining the values for copper, the signal attenuation equation can be simplified as follows:

$$Attenuation(dB) = 20\log e^{-15.1\sqrt{f}z}$$

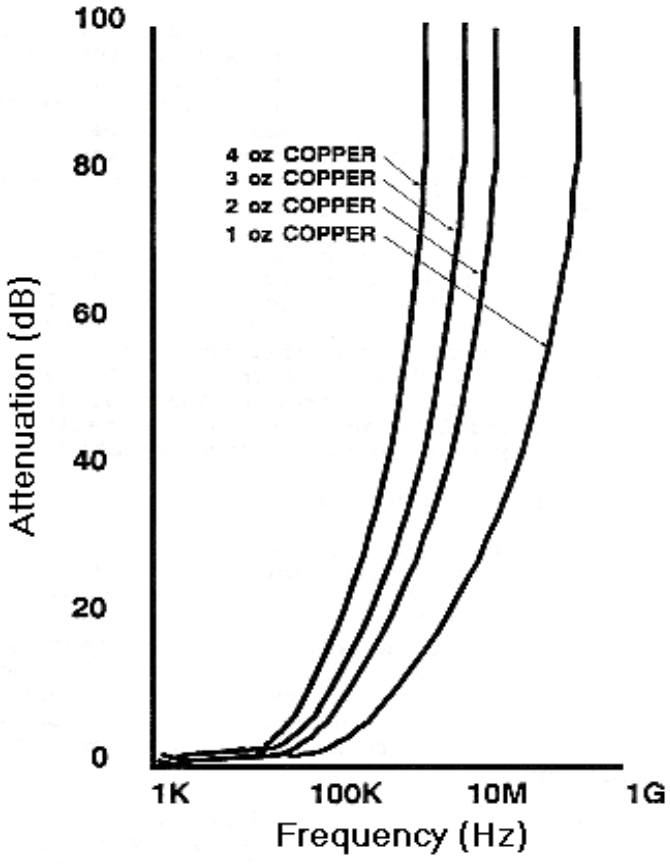


Figure 8-7 Signal Attenuation as a Function of Copper Ground Plane Thickness

Signal attenuation for common copper ground planes are plotted in Figure 8-7. As would be expected, the plots show that thicker foil provides increased attenuation with frequency. As is also apparent, little attenuation is achieved for signals below 1 MHz for any weight copper. This is because of the limitation of capacitive coupling to the ground plane for lower frequencies.

Capacitance Between Traces

The configuration associated with signal and ground plane or grounded trace routing has a significant impact on inter-trace coupling. Coombs (2) has evaluated the interaction of various configurations with the following results shown in Figures 8-7 and 8-8a-b. Pattern 1 of Figure 8-8a-b shows traces laminated between ground planes. Pattern 2 shows multiple layers of traces, one layer above and one layer below the conducting layer, and Pattern 3 shows a single layer of traces without a ground plane.

As shown in Figure 8-9a-b-c, Patterns 1 through 3 were evaluated for inter-trace capacitance under three different conductor and ground trace interconnections. Pattern 3 is included in Configuration 3 as a baseline. The results of the study show interesting

interactions between the various configurations. Note that Pattern 1 and Pattern 2 track very closely, even though Pattern 1 has solid ground planes above and below. Remember that the graphs represent inter-conductor edge coupling only, and do not reflect the effects a solid plane would have in controlling a radiated emission.

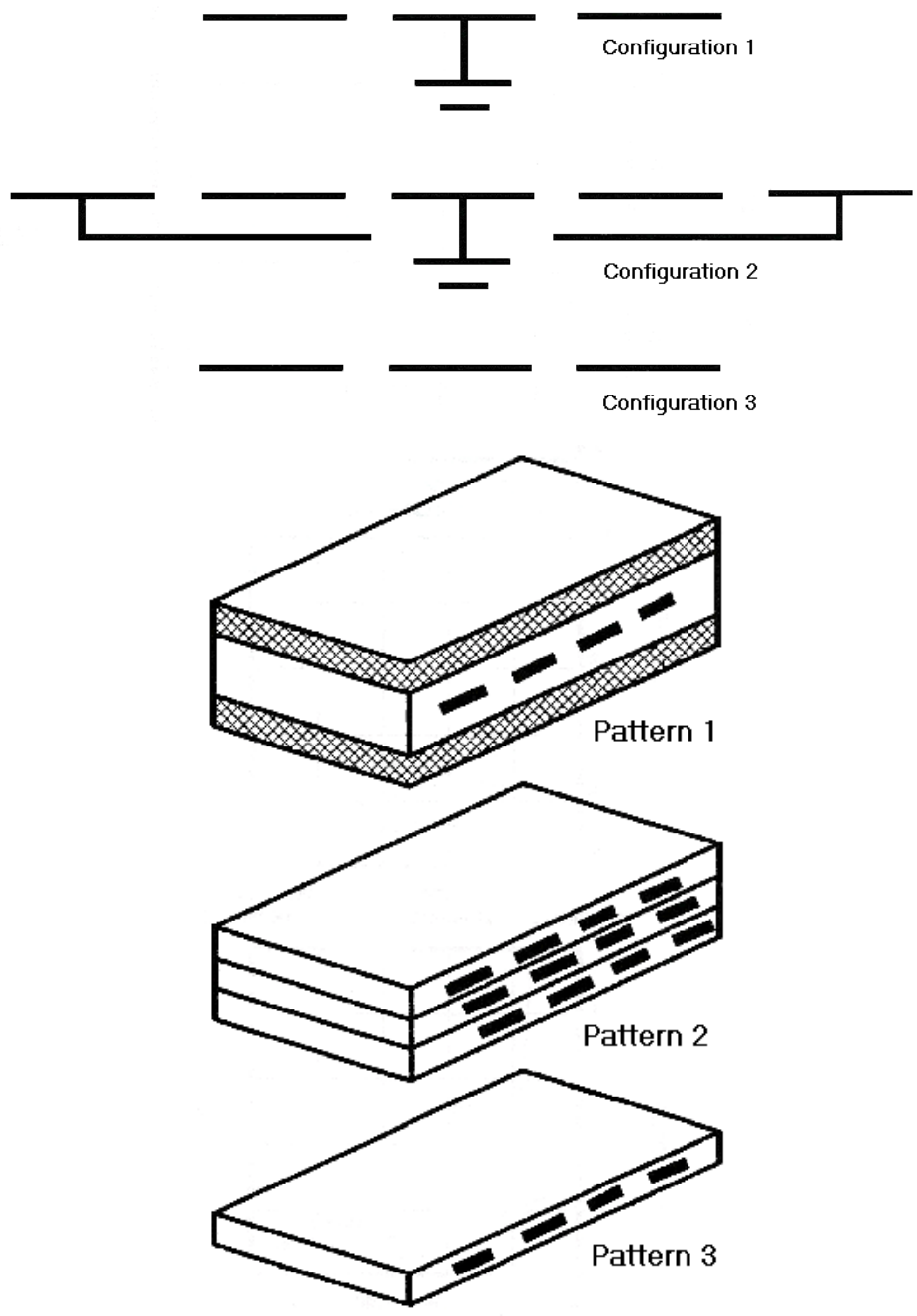
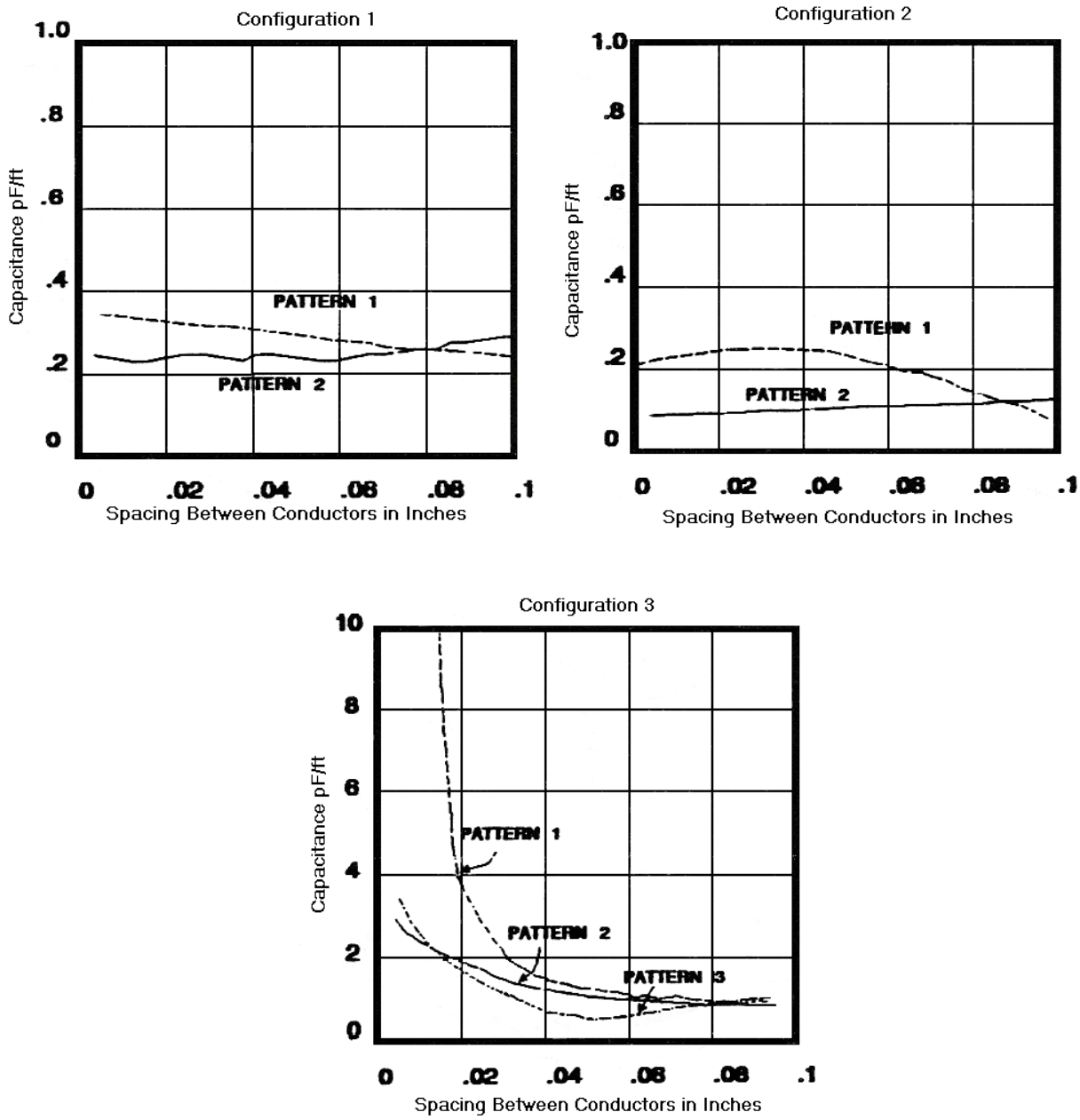


Figure 8-8a-b Trace Patterns & Test Configurations



Figures 8-9a-c Capacitance as a Function of Trace Configuration

Physical Location and Configuration

Regardless of the number of layers on a pc board, short interconnect traces and isolation through circuit nesting are the preferred technique for board layouts. Since the reduced emission characteristics associated with ground planes are the most desirable, multilayer boards with ground planes are normally employed in TEMPEST applications. However, while most standard multilayer applications promote the use of an unbroken

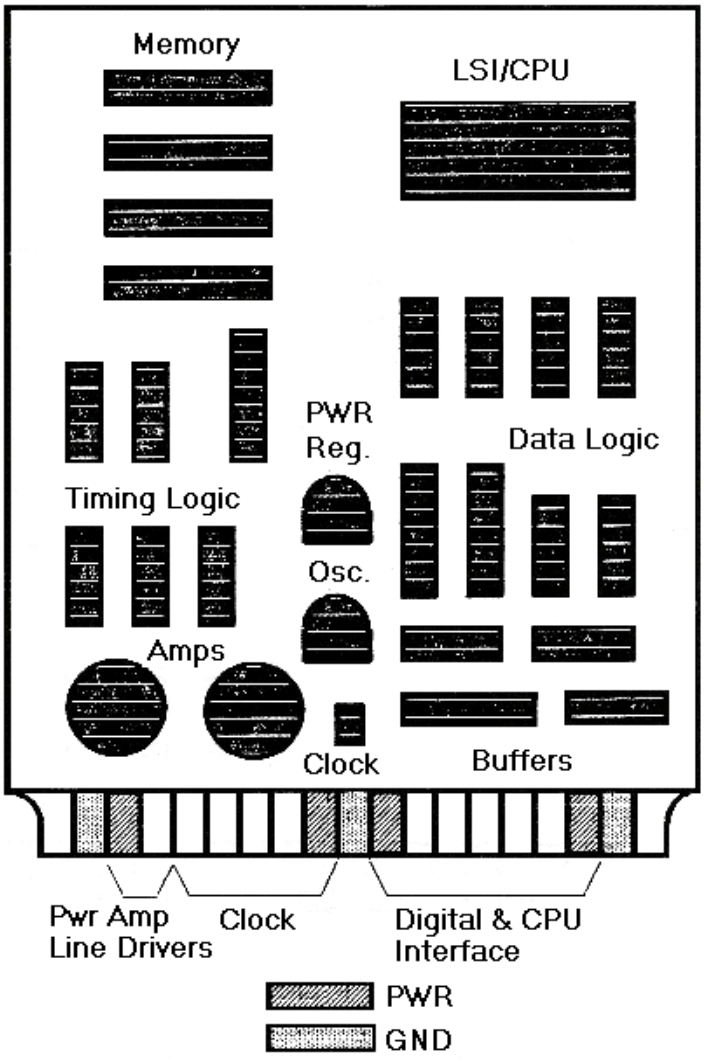


Figure 8-10 Typical PC Board Layout

ground plane, unless a sandwich configuration is to be used, there are instances when breaking the ground plan is extremely beneficial to the TEMPEST designer.

Consider the multilayer pc board layout shown in Figure 8-10. In this case three separate circuit "nests" exist, each containing circuitry of similar sensitivity and emission characteristics. Since 1/0 buffers driving Red lines require the most isolation, they are located closest to the connector, and as far away as possible from higher power amplifiers, and also from noisy oscillators. Figure 8-11a, 8-11b, and 8-11c show the breakout of each individual nest.

Notice that while all grounds are connected together adjacent to the input connector in Figure 8-11, three individual ground planes exist, one for each nest. This is a hybrid single point ground technique for restricting circulating ground currents associated since I/O buffers driving Red lines require the most isolation, they are located closest to the connector, and as far away as possible from higher power amplifiers, and also from noisy oscillators. Figure 11a, 11b, and 11c show the breakout of each individual nest.

While all grounds are connected together adjacent to the input connector in Figure 8-11, three individual ground planes exist, one for each nest. This is a hybrid single point ground technique for restricting circulating ground currents associated with high current power amplifiers from coupling through common mode paths to sensitive circuitry and vice versa. This same technique can be used to isolate ground coupled signals associated with oscillators, such as shown in Figure 8-12. Notice that for both cases shown, the main single point ground for the noisy signal sources is associated with the center ground input connector pin.

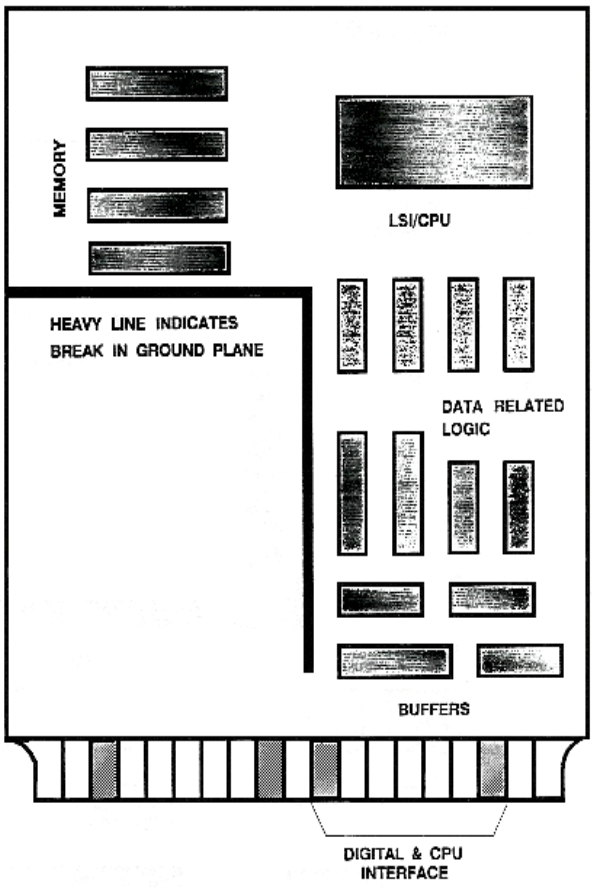


Figure 8-11a Data Logic Nest

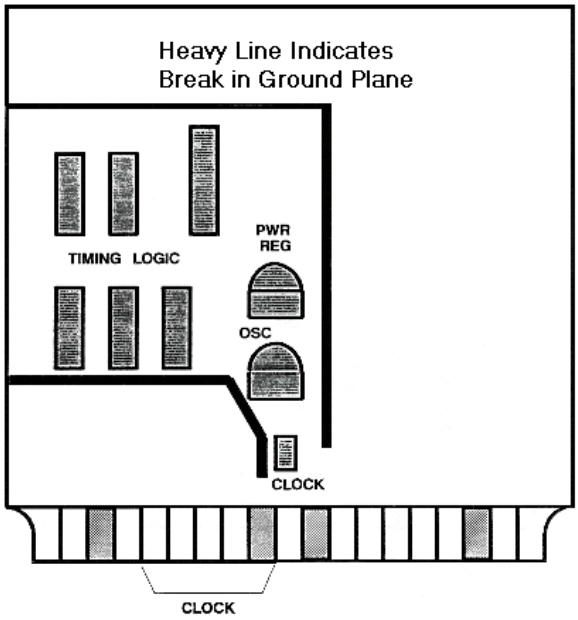


Figure 8-11b Timing & Control Nest

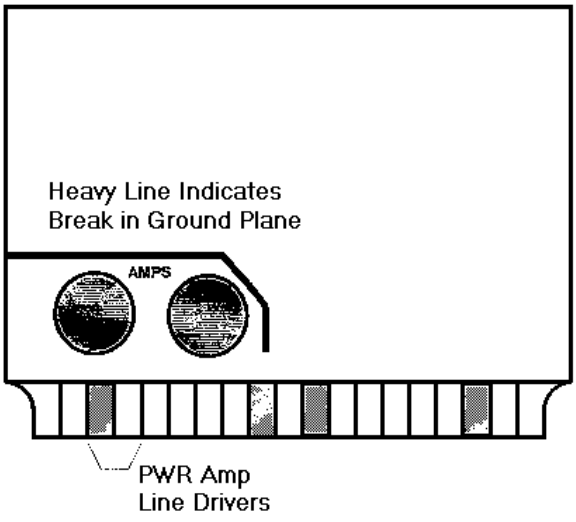


Figure 8-11c Power Amp Nest

A second means of controlling ground noise is shown in Figure 8-13a and 8-13b. In this case, the objective is to minimize the ground loop created by two cards interfacing each other. Ground for each card is provided through the wide and heavy contact area associated with the board ground plane, and does not rely primarily on the inductive wiring associated with a backplane or motherboard power trace for proper interface circuit operation.

Bernard Cooperstein (5) suggests a series of high frequency signal distribution schemes, plus some layout schemes that can cause emission problems on pc cards. His suggestions are shown in Figures 8-14 and 8-15. In addition, he suggests that it is

generally necessary to add a 25 to 30 ohm series resistor at the output of each driver in order to reduce noise, and to also avoid using more then four loads per output.

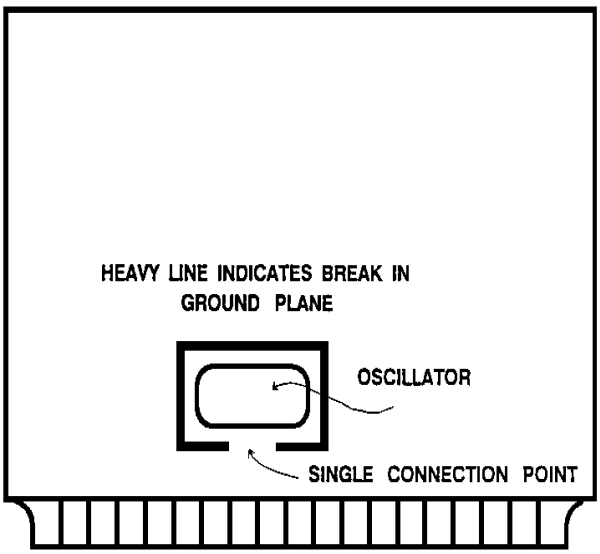


Figure 8-12 Technique for Controlling Oscillator Induced Ground Noise

Board/Bulkhead Separation

If the pc board is adequately suppressed and unwanted emissions are still a problem, carefully examine the interfaces to the card. Figures 13A and B detailed means to reduce Ground inductance in the poser supply rail. Another means of isolating and reducing common mode related board emissions is to provide a second board to isolate the primary board's interfaces. Figure 8-16 shows this approach that is commonly used in situations where very little if any source suppression can be added to an existing card. Bypass and series filtering can be effectively applied on a separate sparsely populated board since ground returns (and ground planes) can be well controlled. It is normally very easy to provide a low inductance multiple ground connection to the separate interface card. In addition to a controlled low impedance ground, ferrites can be added to increase the high frequency impedance between the primary card's load and the interface card, resulting in less energy flowing to the output.

Conclusion

This chapter addressed the initial design of emission controlled printed circuit boards. Again, it is important to stress that problems at the board level normally exist before the TEMPEST engineer becomes involved. In these instances, board and circuit modification rather then re-layout are usually the most cost effective solution to a problem. However, when the opportunity exists for a board re-layout, many simple techniques can be used to effectively reduce emission problems due to board level conditions.

References

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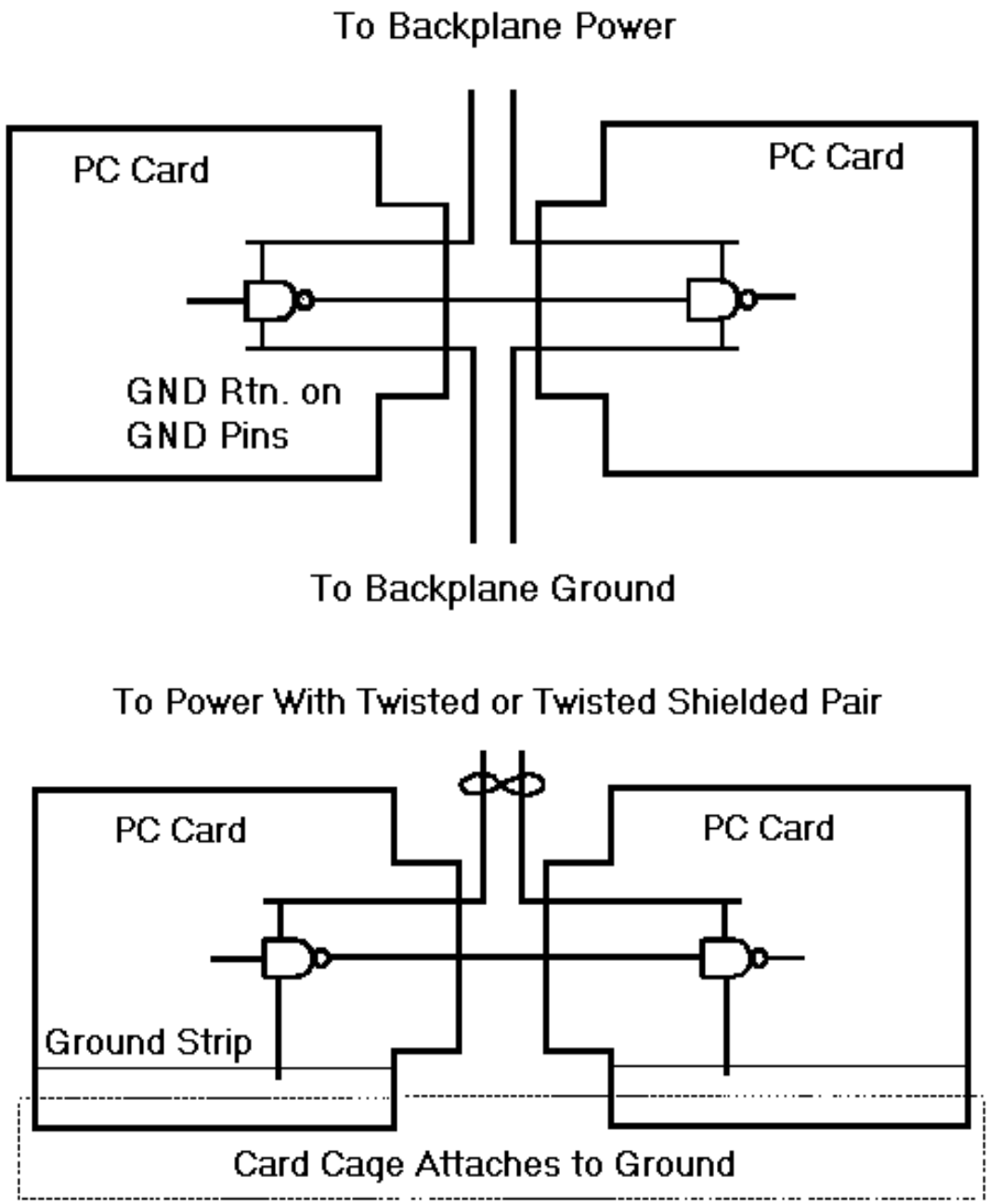

Figure 8-13 Power & Ground Connections for PC Card Mounting System

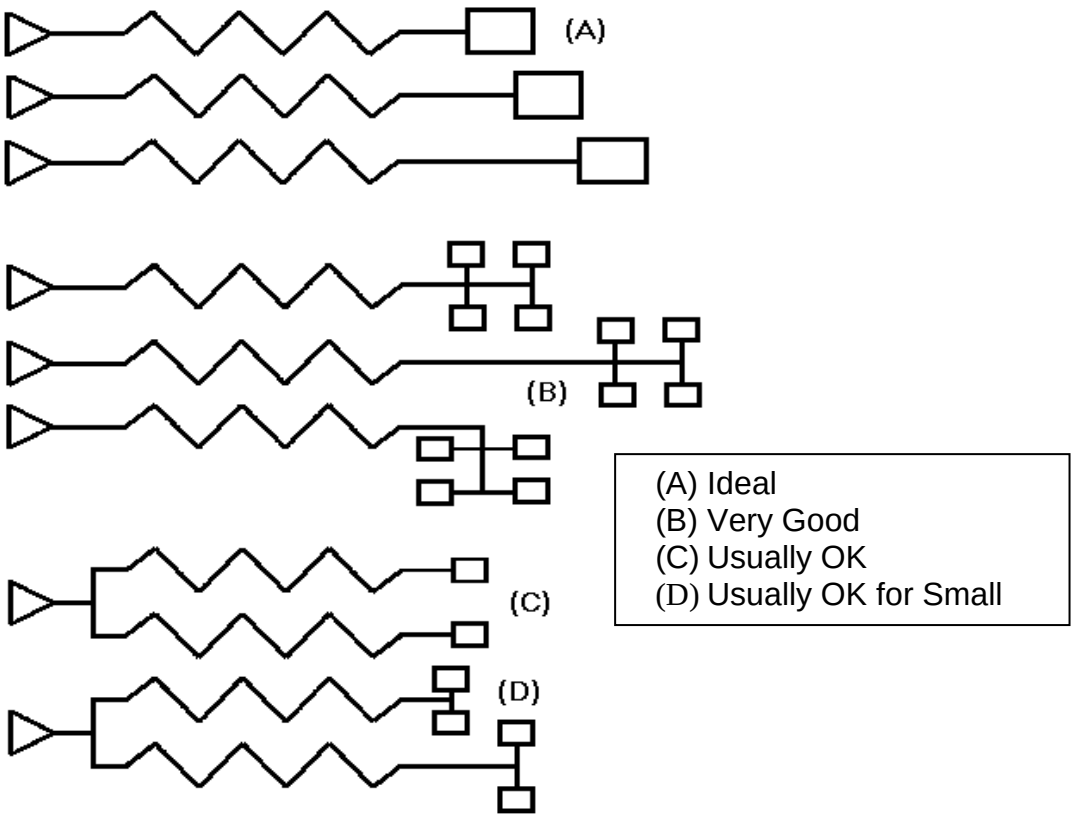

Figure 8-14 Acceptable HF Distribution Schemes

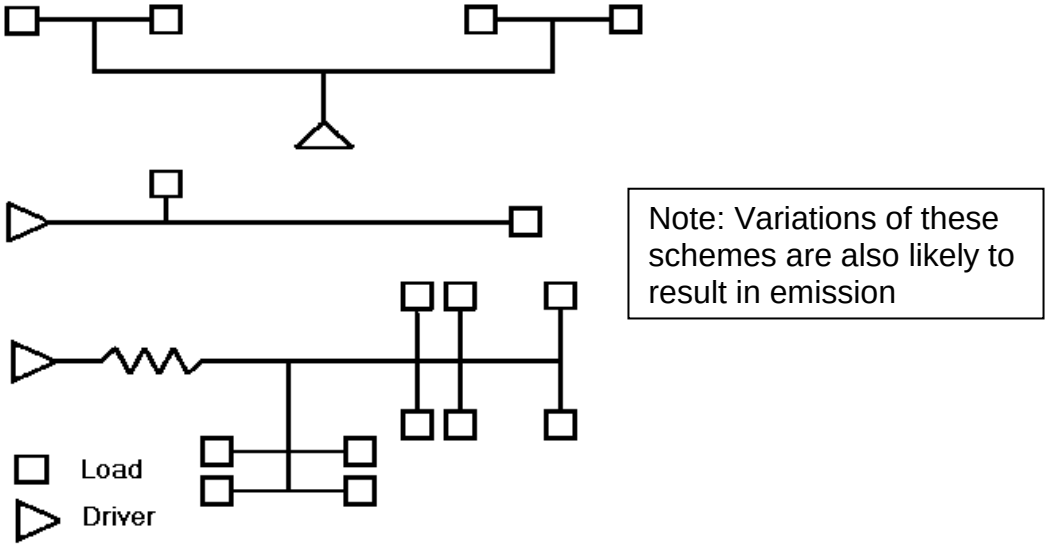

Figure 8-15 Unacceptable HF Signal Distribution

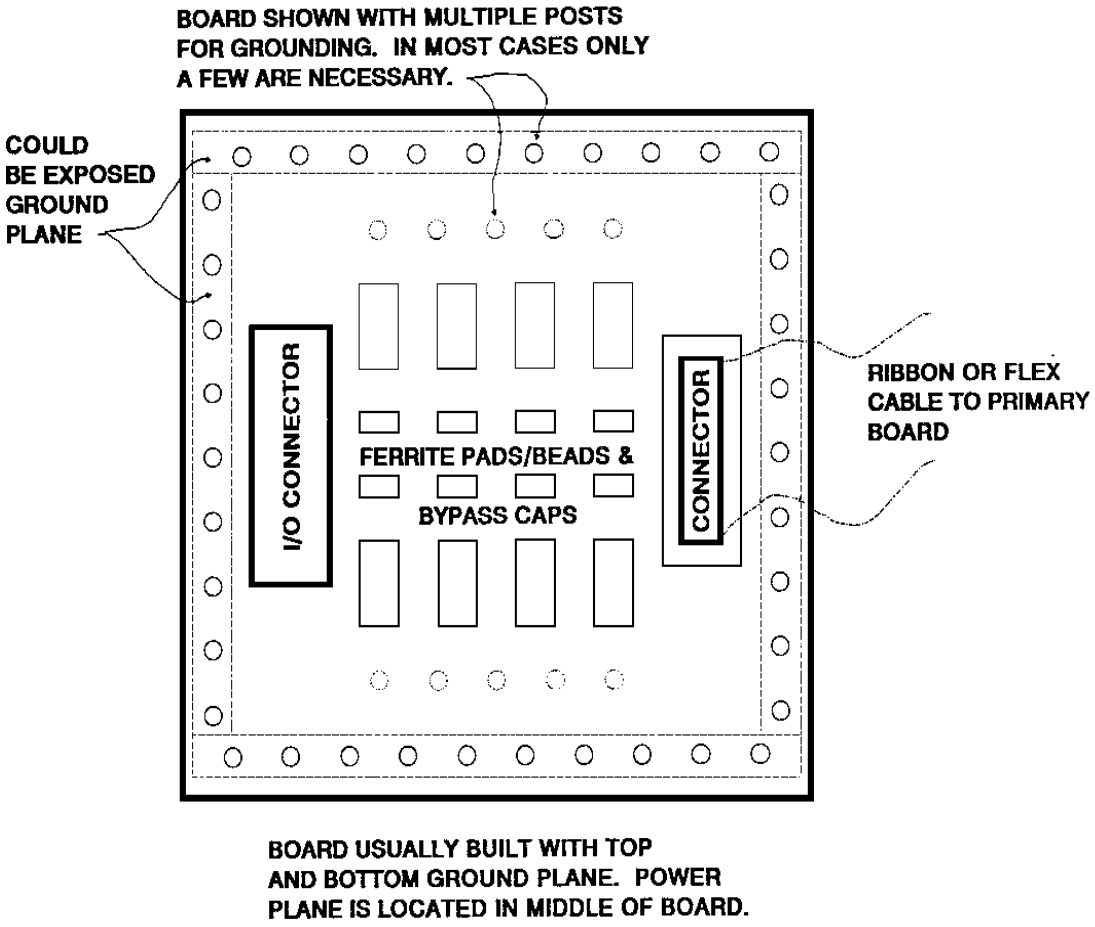

Figure 8-16 Isolated I/O Board